## Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have not been amended.

No new matter has been added.

For example support for the amendments is found in the Specification at paragraph 0020:

## Claim Rejections under 35 USC 112

1. Claims 1-20 stand rejected under 35 USC 112, first paragraph, as failing to comply with the written description requirement.

Examiner alleges that Applicants fail to disclose "a metal silicide layer formed over and electrically connected with the

conductor contact region;" Applicants respectfully note that Examiners new rejection under 35 USC 112, first paragraph in final rejection amounts to piecemeal examination since Applicants have only amended the claim to recite "conductor contact region" versus "contact region".

Nevertheless, Applicants clearly point out in the Specification that there is a conductor barrier layer 14a between the conductor contact region (12) and the metal silicide region 17a (see Figure 3) to provide "electrical connection with the conductor contact region".

See paragraph 0023:

"The blanket conductor barrier layer 14 may be formed of conductor barrier materials as are conventional in the microelectronic product fabrication art, including but not limited to nitrides of metal silicide forming metals such as but not limited to titanium, tungsten, cobalt, nickel, platinum, vanadium and molybdenum. The blanket conductor barrier layer 14 may be formed employing methods as are conventional in the art, to provide the blanket conductor barrier layer 14 of thickness from about 50 to about 500 angstroms. Preferably, the blanket

conductor barrier layer 14 is formed of a titanium nitride conductor barrier material formed to a thickness of from about 100 to about 200 angstroms."

See paragraph 0028:

"Fig. 3 first shows the results of sequentially patterning the partially consumed blanket first doped polysilicon layer 20', the blanket metal silicide layer 17 **and the blanket barrier layer 14 to form a corresponding series of patterned layers comprising a patterned first doped polysilicon layer 20a aligned upon a patterned metal silicide layer 17a in turn aligned upon a patterned barrier layer 14a.**"

Examiner has not explained how one of ordinary skill in the art would not understand Applicants disclosed and claimed invention, "a metal silicide layer formed over and electrically connected with the conductor contact region;"

Examiner argues that Applicants have not shown a metal silicide layer in electrical contact with the conductor contact region. Applicants have not claimed in electrical contact with and therefore do not specifically address this assertion, since that is not what Applicants have claimed. However, Examiner has not pointed out how one of ordinary skill in the art, using terms taken in their ordinary usage, would not understand that a Applicants metal silicide layer is electrically connected to a conductor contact region through an intervening conductor barrier layer.

Examiner has provided no support for the apparent assertion that one of ordinary skill in the art would interpret **electrically connected** to be equivalent to **physically contacting.**

Rather, Examiner is required to interpret that claims as follows:

"Examiner is required to interpret the claims by giving the terms thereof **the broadest reasonable interpretation in their ordinary usage as they would be understood by one of ordinary skill in the art in light of the written specification,** including drawings, **unless another meaning is intended by appellants as established in the written specification,** and without reading into the claims any limitation or particular embodiment disclosed in the specification. *See e.g., In re Morris,* 127 F.3d. 1048, 1054-55, 44 USPQ2d 1023, 1027 (Fed. Cir 1997); *In re Zeltz* (893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Rather, Examiner is attempting to read limitations into Applicants claims that are not intended by Applicants, and further, "**electrically connected**" would not be understood by one of ordinary skill in the art in ordinary usage to require **physical contact.**

See MPEP, 8th Ed, Section 2163 (I) (B)

The fundamental factual inquiry is whether the specification conveys with reasonable clarity to those skilled in the art that, as of the filing date sought, applicant was in possession of the invention as now claimed. See, e.g., *Vas-Cath, Inc.*, 935 F.2d at 1563-64, 19 USPQ2d at 1117.

**ADEQUACY OF WRITTEN DESCRIPTION**
***A. Read and Analyze the Specification for Compliance with 35 U.S.C. 112, para. 1***
Office personnel should adhere to the following procedures when reviewing patent applications for compliance with the written description requirement of 35 U.S.C. 112, para. 1. The examiner has the initial burden, after a thorough reading and evaluation of the content of the application, of presenting evidence or reasons why a person skilled in the art would not recognize that the written description of the invention provides support for the claims. **There is a strong presumption that an adequate written description of the claimed invention is present in the specification as filed,** *Wertheim*, 541 F.2d at 262, 191 USPQ; however, with respect to newly added or claims, applicant should show support in the disclosure for the new or amended claims.

Therefore, Applicants respectfully assert that Examiner has not met the **heavy burden** required to make out a *prima facie* case that Applicants claims (as filed) fail to comply with the written description requirement. Rather, Examiner is unduly narrowly limiting Applicants claim terms by attempting to infuse limitations that are not in Applicants specification into

Applicants claims by narrowly interpreting "electrically connected" as meaning "physically contacting".

Moreover, Applicants amended claim 1 is not new matter since claim 1 was amended from the originally filed claims as follows:

"a metal silicide layer formed over and electrically connected with the conductor contact region;"

Applicants respectfully request withdrawal of Examiner's rejection of Applicants claims as either being new matter or failing to comply with the written description requirement since Examiners new rejection is directed at matter included in the claims as filed.

**Claim Rejections under 35 USC 103**

1. Claim 1-20 stand rejected under 35 USC Section 102(b) as being anticipated by Knall et al. (US 6,420,215).

Knall et al. disclose a **multi-level memory array** that uses "rail stacks" that are formed perpendicular to one another (see Abstract; Figure 1 (items 18, and 16). Knall et al. discloses a

first rail stacks are formed **on an insulator layer (12)** where the rail stack includes **a conductive layer (14) on the insulator layer (12)** where the conductor layer is disclosed **may be a metal silicide** (col 3, lines 14-29) or aluminum or copper, or other metal alloys such as MoW, or highly doped semiconductor or TiN; a **highly doped semiconductor layer (15) is formed on the conductor layer,** where the layer 15 is disclosed may be polysilicon (15), or other semiconductor (col 3, lines 30-36). The conductor and semiconductor (doped polysilicon) layers are then etched (patterned) to form half rail stacks, followed by forming **an anti-fuse layer 20,** which is deposited over the half rail stacks **or** grown selectively **on the upper surface of etched semiconductor layer (15),** where the anti-fuse material is disclosed to be silicon dioxide, silicon nitride, silicon oxynitride, amorphous carbon, and other insulating materials and also teach that an undoped layer of polysilicon (col 3, lines 41-58) may be used as the anti-fuse layer. On top of the anti-fuse layer is formed a highly doped polysilicon layer (21) (opposite in polarity to layer 15) perpendicular to the fuse layer. **Thus, here the conductor layer (14) which is disclosed to be metal silicide is formed on an insulator layer (14).**

In another embodiment (Figure 3), Knall et al. disclose an embodiment which shows three complete levels of the array where the rail stacks 4, 5,, and 6, sandwiched between anti-fuse layer materials (e.g., 51 and 42)) where the rail stacks include a conductor layer (e.g., 46) sandwiched between a highly doped upper semiconductor layer and two doped lower semiconductor layers (44 and 45) (col 5, lines 35-49). **In this case, the conductor layer (e.g., 46) which may be a metal silicide is formed on a semiconductor layer (e.g., 45).**

In another embodiment (Figure 4), Knall et al. disclose forming **two doped semiconductor layers (81 and 82) on a conductor layer (which may be metal silicide)** (80) (col 7, lines 30-38), followed by **formation of an anti-fuse layer** (83)) and formation of a doped semiconductor layer (84) of opposite polarity than **semiconductor layers (81 and 82) on the anti-fuse layer (83)**; all of the above layers are then etched to form **patterned layers** (including the conductor layer (80).

Examiner argues that **it is inherent that every contact region be conductive.** Applicants do not address this assertion

since Applicants have not claimed a conductive contact region but **have claimed a conductor contact region** (i.e., as opposed to a semiconductor contact region).

Moreover, Examiner is mistaken in asserting that Knall et al. disclose a metal silicide layer formed over and electrically connected with a conductor contact region.

Examiner refers to (Figure 1, item 14) where it is clearly shown that the **conductor layer (which may be a metal silicide)** is formed on an insulator layer (12) (see col 3, lines 14-18).

In addition, Knall et al. nowhere teach a **conductor contact region** or a conductor contact region in electrical connection with a metal silicide layer, but rather disclose a **conductor layer which may be a metal silicide** (14, Figure 1) which is (electrically connected by **physical contact with an overlying and/or an underlying semiconductor layer** (Figures 1-6) or is **electrically isolated by an underlying insulator layer** (12-Fig 1).

Thus, Knall et al. fail to teach aspects of Applicants

disclosed and claimed invention including those elements in **bold type**:

"An anti-fuse structure comprising:

a substrate having formed therein a **conductor contact region**;

**a metal silicide layer formed over and electrically connected with the conductor contact region**;

a first doped polysilicon layer formed upon the metal silicide layer;

an anti-fuse material layer formed upon the first doped polysilicon layer; and

a second doped polysilicon layer formed upon the anti-fuse material layer."

As noted above, Knall et al. disclose a conductor (which may be metal silicide) sandwiched between doped semiconductor layers (Figure 3), where a doped polysilicon layer (15) is formed on a conductor layer (14) (e.g., metal silicide) (Fig 2), **which is formed on an insulator (12) or where the conductor (31) is formed**

**on a semiconductor layer (item 30)**; see also Figure 4, where a conductor layer (85) is formed on a semiconductor layer (84).

Nowhere does Knall et al. teach **a metal silicide layer formed over and electrically connected with the conductor contact region.**

Thus even assuming *arguendo*, that it is inherent that a contact region is conductive, Applicants have claimed a **conductor contact region** and Knall et al. nowhere disclose such a feature or a metal silicide in electrical contact with such a feature. Moreover, Knall et al. teach that the term **conductor** is distinct from **semiconductor**.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

With respect to **claims 4, 9, 14, and 19** Examiner is mistaken

in asserting that Knall et al. teach "wherein a doped polysilicon layer is not formed interposed between the contact region and the metal silicide layer".

As noted above, Knall et al. teach a conductor layer (which may be metal silicide) sandwiched between an insulator layer (WITH NO CONDUCTOR CONTACT REGIONS) and a semiconductor layer or sandwiched between two semiconductor layers.

With respect to claims 5, 10, 15, and 20, Examiner is mistaken in asserting that Knall et al. teach "further comprising a barrier layer formed interposed between the contact region and the metal silicide layer and contacting the metal silicide layer."

Examiner now refers to the an insulator layer (described at col 5, lines 35-47) which discusses the embodiment in Figure 3, where the space (50) between conductor and semiconductor structures is filled with an electrically insulating dielectric rather than a barrier layer (to provide electrical connection with the metal silicide) as would be understood by one of ordinary skill in the art in light Applicants specification and claims.

"Examiner is required to interpret the claims by giving the terms thereof **the broadest reasonable interpretation in their ordinary usage as they would be understood by one of ordinary skill in the art in light of the written specification,** including drawings, **unless another meaning is intended by appellants as established in the written specification,** and without reading into the claims any limitation or particular embodiment disclosed in the specification. *See e.g., In re Morris,* 127 F.3d. 1048, 1054-55, 44 USPQ2d 1023, 1027 (Fed. Cir 1997); *In re Zeltz* (893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

**Examiner Arguments**

Examiner argues that the addition of "conductive" to contact region does not meaningfully change the scope of the claims "because it is inherent that every contact region be conductive". However, Examiner ignores the fact that Applicants have claimed a **conductor contact region**, and that Knall et al. do not disclose any sort of contact region, but rather disclose a metal silicide layer **(conductor)** in **physical contact with an underlying insulator or a semiconductor (not a conductor).**

**Conclusion**

The cited reference, Knall et al. does not produce Applicants disclosed and claimed invention and is therefore insufficient to make out a *prima facie* case of obviousness.

Based on the foregoing, Applicants respectfully request reconsideration of their claims and submit that Applicants Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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